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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,763	11/08/2001	Junsong Li	SC11804TS	3072

23125 7590 04/26/2005

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EXAMINER	
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ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,763	LI ET AL.	
	Examiner	Art Unit	
	Tony M Jacobson	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13 and 15-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 11** is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 11 merely recites an intended use for the apparatus, which does not serve to limit the structure of the apparatus. The courts have ruled, "Such use or process differences properly are not included in such an apparatus claim." (In re Sebald 122 USPQ 527 – see #2).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 1 and 25** are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a multiplier for multiplying the input signal by "a signal having a predetermined cosine value equal to 2Cos (2πX20000t) where t is time" (as disclosed at page 10, lines 17-19 of the specification), does not reasonably provide enablement for "a multiplier for multiplying a predetermined value by the input signal to generate an intermediate signal wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a lower frequency than the pilot signal component in the input signal" as claimed. The specification does

not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Applicant has not disclosed how a general "value" (or any value other than 2cos[40,000π]) can be used to practice the invention.

4. **Claims 18 and 21** are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for multiplying the input signal by "a signal having a predetermined cosine value equal to 2Cos (2πx20000t) where t is time" (as disclosed at page 10, lines 17-19 of the specification), does not reasonably provide enablement for "multiplying a predetermined value by the input signal to generate an intermediate signal, the input signal having a pilot signal component that is also in the intermediate signal but reduced in frequency in the intermediate signal" as claimed. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. Applicant has not disclosed how a general "value" (or any value other than 2cos[40,000π]) can be used to practice the invention..

5. **Claims 5, 6, 12, and 13** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

6. **Claim 5** recites "A decoder as in claim 1, wherein said first decimator, second decimator and third decimator each decimate by approximately a same decimation factor." Applicant has not disclosed an embodiment of the invention in which the first decimator (i.e., 306 of Fig. 3), decimating the sum (L+R) signal (as recited at lines 6-9 of claim 1), or the third decimator (i.e., 312 or 324 of Fig. 3), decimating a first of the pair of quadrature signals (as recited at lines 35-36 of claim 1), each decimate by approximately a same decimation factor. Claim 1 recites that the "second" decimator decimates the pilot signal component to a sampling rate "no more than substantially 12K samples per second", while the sum (L+R) signal decimated by decimator 306 and the quadrature signals decimated by decimator 312 or 324 all have signal bandwidths of about 15 kHz, which restricts decimation to a sampling rate of at least 30 kHz; since Applicant's disclosure shows that each of these decimators receive signals with a same initial sampling rate (e.g., 240 kS/s), attempting to decimate the sum signal (at 306 of Fig. 3) or the quadrature signals (at 312 or 324 of Fig. 3) by the same decimation factor applied to the frequency-reduced pilot signal component (at 374 of Fig. 3) would result in aliasing of higher frequency components (above 6 kHz) of these signals. Thus, Applicant has not disclosed the invention in such a way as to enable one of ordinary skill in the art to make and use the invention as claimed. The following prior art rejections assume Applicant intended to recite, "... said first decimator, third decimator, and **fourth decimator** ...", consistent with claim 1 and the specification.

7. **Claim 6** recites, "a fourth decimator coupled between the second low pass filter and the phase angle estimation means, the fourth decimator decimating the pilot signal component." Applicant has claimed in claim 1 a "second" decimator having a predetermined decimation factor and coupled to the second low pass filter, the second decimator reducing a sampling rate of the pilot signal component (at lines 21-23 of claim 1, presumably 374 of Fig. 3); and has not disclosed an embodiment of the invention in which an additional decimator is coupled between the second low pass filter (presumably 372 of Fig. 3) and the phase angle estimation means (presumably 376 of Fig. 3). Therefore, the claimed subject matter was not described in the specification in such a way as to enable one of ordinary skill in the art to make and use the invention.

8. **Claim 12** recites, "A decoder as in claim 1, wherein the predetermined value is approximate to, but not equal to, a frequency of the pilot signal component in the input signal." Applicant has not disclosed how the predetermined "value" is approximate to, but not equal to, a frequency of the pilot signal component in the input signal in such a way as to enable one of ordinary skill in the art to make and use the invention. The term "value" is generally used to refer to a single value, such as a particular voltage level, rather than a specific time-varying function (i.e., a predetermined sequence of values). Although Applicant has described at page 10, lines 17-19 of the specification that a "cosine value equal to $2\text{Cos}(2\pi x20000t)$, where t is time" is multiplied by the input signal in multiplier 370, the limitation claimed is open to a number of interpretations, such as multiplying the input signal by a constant value of approximately 19,000 (a

frequency of the pilot signal component in the input signal, in Hertz), multiplying the input signal by a constant value of approximately 38,000π (a frequency of the pilot signal component in the input signal, in radians/sec), or multiplying the input signal by a constant value of approximately 2π·19,000/240,000 (which equals approximately 0.497 [radians/sample] and is a frequency of the pilot signal component in the input signal, relative to the sampling rate of 240k Samples/second, according to a common definition of frequency in digital signal processing). While the specification discloses how a **sinusoidal signal** that is a periodic function of time ("cosine value equal to 2Cos[2πx20000t]", **having a frequency** of 20,000 Hz, which is approximate to, but not equal to, a frequency of the pilot signal component in the input signal) is multiplied by the input signal, the specification does not describe how a general "value" that is multiplied by the input signal is approximately equal to a frequency of the pilot signal component in the input signal, in such a way as to enable one of ordinary skill in the art to make and use the invention as claimed.

9. **Claim 13**, containing the limitation "wherein the predetermined value is within 3 kilohertz of the frequency of the pilot signal component in the input signal", is rejected by the same reasoning applied to claim 12, stated above.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. **Claims 1, 6, 16-18, and 25** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. **Claim 1** recites the limitation "the sixth low pass filter that processes the output signal containing a difference of left channel information and right channel information" in lines 51-53 of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim make no prior mention of a "sixth low pass filter that processes the output signal containing a difference of left channel information and right channel information"; and, while a "sixth low pass filter" is previously recited, it is unclear whether this is the same sixth low pass filter to which reference is currently made. Also, it is unclear whether the phrase "that processes the output signal containing a difference of left channel information and right channel information" is intended to limit or merely to identify the recited "sixth low pass filter".

13. **Claim 6** recites the limitation "the phase angle estimation means" in lines 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim. No prior mention is made of a "phase angle estimation means". The following prior art rejections assume Applicant intended to recite "digital phase lock loop" as in amended claim 1.

14. **Claim 6** also recites, "a fourth decimator coupled between the second low pass filter and the phase angle estimation means, the fourth decimator decimating the pilot signal component." Claim 1, upon which claim 6 depends has already recited "a fourth decimator coupled to the fourth low pass filter for decimating a second of the pair of quadrature signals to provide a second quadrature mixer output" (at lines 37-39 of the claim, presumably in reference to 312 or 324 of Fig. 3) and "a second decimator having a predetermined decimation factor and coupled to the second low pass filter, the second decimator reducing a sampling rate of the pilot signal component (at lines 21-23 of the claim, presumably referring 374 of Fig. 3). The claiming of two distinct "fourth decimators" renders the claim ambiguous and, therefore, indefinite. (It appears that this claim refers to the "second decimator" recited at lines 21-23 of claim 1 [presumably 374 of Fig. 3], but that the relationship of this claim to amended claim 1 was not fully considered by Applicant.)

15. **Claim 16** recites "A decoder as in claim 6, wherein said fourth decimator reduces sampling rate of the intermediate signal by a factor of 20." As claim 6 has recited two

distinct "fourth decimators" as described above, it is unclear to which of these fourth decimators reference is being made. It is assumed in the prior art rejections that follow that Applicant intended to refer to the "second decimator" recited at lines 21-23 of claim 1, rather than a "fourth decimator".

16. **Claim 17** recites the limitation "said phase angle estimation means" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim. No prior mention is made of a phase angle estimation means. The following prior art rejections assume Applicant intended to recite "digital phase lock loop" as in amended claim 1.

17. **Claim 17** also recites, "A decoder as in claim 1, wherein said phase angle estimation means operates at a frequency less than one tenth the predetermined frequency of the input signal." First assuming Applicant intended to recite "digital phase lock loop" rather than "phase estimation means", as noted directly above, the limitation "a frequency less than one tenth the predetermined frequency of the input signal" is indefinite because, as the examiner points out below in regard to the rejection of claim 1 under 35 USC 103(a), the input signal of Applicant's decoder, as well as that of the decoders of Vogt et al., and Noeske et al., contains a number of signal components (e.g., the 19-kHz pilot signal component and the 38-kHz suppressed carrier of the difference (L-R) signal component) that each have a predetermined frequency, and the input sampling rate also constitutes a "predetermined frequency" of the input signal.

Since it is not clear to which of these (or possibly another) fixed frequency of the input signal claim 17 refers, the scope of the claim cannot be determined, and the claim is thus indefinite.

18. **Claim 18** recites "... a first output that contains a sum of left channel and right channel information" at lines 4-5; "... a second output that contains a difference of left channel information and right channel information" at lines 16-18; and "... first and second outputs of quadrature mixers ..." at lines 19-20; then recites at line 22, "blending the first output and the second output to provide a left channel signal and a right channel signal ...". As two distinct first outputs and two distinct second outputs are recited, it is unclear to which "first output and second output" the blending limitation refers.

19. **Claim 25** is directed to two classes of statutory subject matter. The claim attempts to embrace both an apparatus or machine and a process. This is precluded by the language of 35 U.S.C. 101, which sets forth the statutory classes of invention in the alternative only. While a single patent may include claims directed to more than one statutory class of invention, no basis exists for permitting a combination of two separate and distinct classes of invention in a single claim. The claiming of two statutory classes of invention in a single claim is ambiguous and renders the claim indefinite. Claim 25 is presented as an apparatus claim (a decoder), and most of the limitations describe elements of the apparatus; however, the claim recites the process step, "decimating the

pilot signal component by a decimation factor of substantially twenty and reducing a sampling rate of the pilot signal component to no greater than substantially twelve thousand samples per second" at lines 9-11.

Claim Rejections - 35 USC § 101

20. **Claim 25** is rejected under 35 U.S.C. 101 because the claimed invention is directed to two classes of statutory subject matter. The claim attempts to embrace both an apparatus or machine and a process. This is precluded by the language of 35 U.S.C. 101, which sets forth the statutory classes of invention in the alternative only. While a single patent may include claims directed to more than one statutory class of invention, no basis exists for permitting a combination of two separate and distinct classes of invention in a single claim. (See related 35 USC § 112, second paragraph rejection above.)

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **Claims 1-6, 8-13, and 15-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (US 5,442,709) in view of Noeske et al. (US 6,351,631), Eory (US 5,832,043), and Kawamura (US 5,202,925).

23. Regarding **claim 1**, Vogt et al. discloses in Fig. 1, a decoder having an input signal (1) with a predetermined frequency (the sampling frequency, the frequency of a pilot signal component, and the frequency of a suppressed 38 kHz subcarrier are all predetermined, as in Applicant's invention; other varying, non-predetermined frequency components are also present, as in any conventional FM stereo multiplexed signal) and providing a left channel signal and a right channel signal, comprising:

a multiplier (15 or 15a) for multiplying a predetermined "value" (16) by the input signal to generate an intermediate signal, wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a predetermined lower frequency than the pilot signal component in the input signal (column 4, lines 20-36);

a "second" low-pass filter (18 or 17) for receiving the intermediate signal and providing the pilot signal as an output;

a "second" decimator (19 or 20) having a predetermined decimation factor and coupled to the "second" low pass filter, the "second" decimator reducing a sampling rate of the pilot signal component;

a [correction signal generating network] (21 – see Fig. 2) for determining an approximate phase of the pilot signal component and generating at least one trigonometric function (G38c and G38s) using the approximate phase of only the pilot signal component, the at least one trigonometric function representing a phase angle needed to correct phase error associated with an output signal that contains a difference of left channel information and right channel information (see column 3, line 43 –column 4, line 4 and column 4, line 18 –column 5, line 18);

quadrature mixer means (2, 3, and 14) coupled to the input signal for shifting the input signal from the predetermined frequency to a lower frequency by forming a pair of quadrature signals (column 3, lines 18-56);

means (4 and 5 of Fig. 1) for using the at least one trigonometric function (G38c, G38s), the first quadrature mixer output (Imr1), and the second quadrature mixer output (Imr2) to generate a phase-aligned output signal (L-R, at 6) that contains a difference of the left channel information and the right channel information;

and means (7-11) for using the output signal that contains a sum of left channel information and right channel information and using the output signal that contains a

difference of left channel information and right channel information to generate the left channel signal (12) and the right channel signal (13).

Vogt et al. do not disclose the following elements presently claimed:

a "first" low-pass filter for low-pass filtering the input signal to provide a "first" filter output;

a "first" decimator coupled to the "first" low-pass filter for decimating the "first" low-pass filter output to reduce a sampling frequency of the input signal, the "first" decimator providing an output signal that contains a sum of left channel information and right channel information;

that the sampling rate of the pilot signal component is reduced to [specifically] no more than substantially 12k samples per second;

that the correction signal generating network (21) is a phase lock loop;

a "third" low-pass filter and a "fourth" low-pass filter each respectively low-pass filtering a predetermined one of the pair of quadrature signals;

a "third" decimator coupled to the "third" low-pass filter for decimating a first of the pair of quadrature signals to provide a first quadrature mixer output;

a "fourth" decimator coupled to the "fourth" low-pass filter for decimating a second of the pair of quadrature signals to provide a second quadrature mixer output; nor

that the means for using the output signal that contains a sum of left channel information and right channel information and using the output signal that contains a difference of left channel information and right channel information to generate a left

channel signal and a right channel signal comprises a "fifth" low-pass filter and a "sixth" low-pass filter that are dynamically and separately controlled low-pass filters, the "fifth" low-pass filter processing the output signal that contains sum of left channel information and right channel information and having its bandwidth varied after first varying bandwidth of the "sixth" low-pass filter that processes the output signal containing a difference of left channel information and right channel information, an amount of bandwidth adjustment being increased in proportion to detected increased signal distortion.

Although Vogt et al. do not disclose ("first", "third", and "fourth") low-pass filters and associated ("first", "third", and "fourth") decimators filtering and decimating the input signal and the pair of quadrature signals output by the quadrature mixer means, Vogt et al. do disclose low-pass filters 17 and 18 and corresponding decimators 19 and 20 low-pass filtering and decimating the pair of "intermediate" quadrature signals produced by the multipliers 15 and 15A, which has the pilot signal component at a lower frequency than the frequency of the pilot signal component in the input signal. Vogt et al. disclose at column 4, lines 33-40 that because the frequency of the frequency-reduced quadrature pilot signals output from the multipliers (15 and 15A) (less than about 70 Hz) is much lower than that of the original pilot frequency, the sampling rate is reduced at decimators 19 and 20, which saves significant expense in the following network (21). Vogt et al. also disclose at column 4, lines 26-64 that correction signal generating network (21) functions to receive signals $SPC1_n = \sqrt{A} \cdot cos(\alpha)$ and $SPC2_n = \sqrt{A} \cdot sin(\alpha)$, which represent the cosine and sine, respectively, of the phase error of the pilot signal

component of the input signal with respect to the phase of the 19-kHz reference pilot signal obtained from table 16 (column 3, lines 51-53), and to generate in response thereto the signals G38c = *cos*(2α) and G38s = *sin*(2α), which represent the cosine and sine, respectively, of the phase error of the suppressed carrier of the DSBSC (double-sideband suppressed-carrier) modulated difference (L-R) signal component of the composite input signal with respect to the 38-kHz reference carrier obtained from table 14 (column 3, line 43 –column 4, line 6).

Phase lock loops were notoriously well known in the art at the time the present invention was made, for performing this same general function (i.e., receiving a sinusoidal input signal (or quadrature-phased signal pair) of a particular frequency and phase, and generating in response thereto one or more phase-coherent sinusoidal output signals having frequency and phase that are an integer multiple of the frequency and phase of the input signal). Also, it was notoriously well known in the art at the time the present invention was made to employ (digital or analog, as appropriate) phase lock loops in conventional multiplex stereo decoders that do not employ frequency reduction of the difference signal component and pilot component of the composite input signal to near baseband by mixing with reference carriers generated by free-running (with respect to the actual frequencies and phases of input signal components) oscillators as in Vogt et al. and the instant invention.

Noeske et al. disclose in Figs. 2 and 4 embodiments of a carrier generating arrangement for demodulating a digital stereo multiplex signal in an FM radio receiver, comprising a digital PLL (10) for locking to the frequency of a pilot signal component of

a composite input signal and thereby generating a pilot phase signal (φ) that is applied to "second value allocator" 20, wherein it is multiplied by a factor of 2 at frequency multiplier 22, adjusted by correcting device 23 to offset unequal delays in the various signal paths, and applied to "angle table" 24 (a ROM table of sine or cosine function values) to form a sinusoidal output signal that is phase-coherent to the received pilot signal component and at twice the frequency of the pilot signal component. The thus-generated sinusoidal signal is then applied to multiplier 21 to perform coherent demodulation of the DSBSC-modulated difference (L-R) signal component of the composite input signal. (See column 2, line 54 –column 3, line 46 and column 4, lines 39-44.) Noeske et al. also disclose (particularly in the embodiment of Fig. 4) several filtering and decimation stages (19.2, 19.3, 40.1, 40.2, and 50) to reduce the sampling rate at each stage as much as possible (while processing each signal component at the frequency at which it naturally occurs in the baseband composite multiplex signal), and discloses at column 5, lines 20-32 that clock rate reduction (by means of decimation) reduces the complexity of the required filters and allows a individual DSP processors to provide increased functionality.

Specifically, with regard to the instant claims, Noeske et al. disclose in Fig. 2:

a "first" low-pass filter (comprised in decimation filter 19 – see column 3, lines 24-27) for low-pass filtering the input signal to provide a "first" filter output;

a "first" decimator (19) coupled to the "first" low-pass filter for decimating the "first" low-pass filter output to reduce a sampling frequency of the input signal, the "first"

decimator providing an output signal that contains a sum of left channel information and right channel information (column 3, lines 24-27); and

a digital phase lock loop (10) for determining an approximate phase of the pilot signal component and generating at least one trigonometric function using the approximate phase of only the pilot signal component, the at least one trigonometric function representing a phase angle needed to correct phase error associated with an output signal that contains a difference of left and right channel information and right channel information (column 2, line 54 –column 3, line 46); and

a low-pass filter and decimator (40 – see column 3, lines 42-45) filtering and reducing the sampling rate of the difference signal (L-R) component following frequency transposition to baseband by mixer 21 (similar to the function of claimed "third" and "fourth" low pass filters and decimators).

Noeske et al. do not disclose that the pilot signal component or the DSBSC-modulated difference signal (L-R) component are mixed with fixed-frequency reference carriers to reduce their frequencies prior to processing, as taught by Vogt et al. and the present invention.

Eory discloses details of a digital phase locked loop (DPLL) that generates a quadrature-phased pair of sinusoidal signals (a complex rotating vector signal) that is phase-coherent with a quadrature-phased carrier signal pair (a complex rotating vector carrier signal) that has been frequency transposed to approximately 0 Hz, and thus may have a positive or negative frequency (rotating clockwise or counterclockwise in the complex plane), depending on indefinite factors, such as uncertainty in the actual local

oscillator frequencies used to transpose the signal frequency. (See column 1, line 64 – column 2, line 37.) While Eory generally discloses that the DPLL is used to correct frequency and phase errors of a near-zero IF (intermediate frequency) signal in a radio receiver, one of ordinary skill in the art at the time the present invention was made would have recognized that the teaching is applicable to phase tracking of any near-zero-Hz complex carrier signal.

In view of the teachings of Noeske et al. and Eory, as described above, and the common practice in the art of employing phase-locked loops to generate one or more phase-coherent output signals at multiples of the frequency of an input signal (the function of the correction signal generating network (21) of Vogt et al., as disclosed at column 4, lines 18-64, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to substitute a phase-locked loop, constructed as generally taught by Eory and including a "second value allocator" (double-frequency sine/cosine generator) as taught by Noeske et al., for the arrangement of Fig. 2 of Vogt et al. to perform the function of doubling the phase error of the reference pilot carrier to form a quadrature-phased phase correction signal pair to correct the phase error of the difference signal (L-R) component in the circuit of Fig. 1 of Vogt et al. as a design choice or in order to avoid the prior art.

Also, according to the general teachings of Noeske et al., it would have been obvious to one of ordinary skill in the art to employ low-pass filters and associated decimators wherever practical to reduce the bandwidth and sampling rate of each signal as much as practical in order to obtain improved operating efficiency as described by

Noeske et al. at column 5, lines 24-32 and by Vogt et al. at column 2, lines 36-38 and column 4, lines 33-36. Specifically, it would have been obvious to provide a "first" low-pass filter for low-pass filtering the input signal to provide a "first" filter output and a "first" decimator coupled to the "first" low-pass filter for decimating the "first" low-pass filter output to reduce a sampling frequency of the input signal, the "first" decimator providing an output signal that contains a sum of left channel information and right channel information (as taught by 19 of Fig. 2 of Noeske et al.); and "third" and "fourth" low-pass filters and associated decimators filtering and decimating each of the pair of quadrature signals (Imr 1 and Imr 2) generated by the quadrature mixer comprising reference carrier generator 14 and multipliers 2 and 3 of Fig. 1 of Vogt et al. (as fairly suggested by elements 40 and 50 of Noeske et al.)

Further, although Vogt et al. do not disclose a specific decimation factor or resultant reduced sampling rate of decimators 19 and 20, Vogt et al. disclose at column 4, lines 26-28 that low-pass filters 17 and 18 of Fig. 1 have a limit frequency of about 70 Hz; thus, it would have been obvious to one of ordinary skill in the art to reduce the sampling rate to any rate that is at least twice that frequency (140 samples per second, which is "no more than substantially 12k samples per second") according to the well-known sampling theorem.

Kawamura discloses in Fig. 3, an FM stereo receiver having an improved automatic reception control (ARC) system and method. Kawamura discloses that the circuit improves on the prior-art circuit of Fig. 7, which has, as part of means for using a signal that contains a sum of left-channel information and right-channel information

(main signal S_M) and using a signal that contains a difference of left-channel information and right-channel information (sub-signal S_S) to generate a left-channel signal and a right-channel signal (S_L and S_R), a variable high-cut (low-pass) filter (2) under the control of high-cut control circuit (8) dynamically controlling the bandwidth of a main signal S_M (containing a sum of left-channel information and right-channel information) controlling the high-frequency content of that signal in response to received signal conditions (signal strength) and a variable attenuation circuit (3) under the control of separation control circuit (3A) dynamically controlling the amplitude of a sub-signal S_S (containing a difference of left-channel information and right-channel information) in response to received signal conditions (signal strength). (See column 1, lines 8-42.) The improvement is made by substituting a second high-cut (low-pass) filter (5 of Fig. 3) for the variable attenuation circuit (3) of Fig. 7, still under the dynamic control of a separation control circuit (now 5A). (See column 2, lines 15-23.) Kawamura discloses at column 1, lines 60-64 that the separation control is effected when the received signal strength level is within the range of, for instance, from 45 dBμV to 25 dBμV (decibels referenced to 1 microvolt), whereas the frequency control is carried out when the received signal strength is less than 35 dBμV.

Thus, the improved circuit of Fig. 3 comprises, with regard to the instant claims: a "fifth" high-cut (low-pass) filter (2) and a "sixth" high-cut (low-pass) filter (5) that are dynamically and separately controlled low-pass filters, the "fifth" low-pass filter processing the (output) signal that contains a sum of left-channel information and right-channel information and having its bandwidth varied after first varying bandwidth of the

"sixth" low-pass filter that processes the output signal containing a difference of left-channel information and right-channel information, an amount of bandwidth adjustment depending being increased in proportion to detected increased signal distortion. (For a decreasing signal strength, separation control 5A will reduce the bandwidth of the "sixth" low-pass filter (5) when the signal strength reaches a level of 45 dBμV; then, after the signal strength is further reduced to a level below 35 dBμV, high-cut control circuit 8 will reduce the bandwidth of the "fifth" low-pass filter (2) as described at column 1, lines 60-64.) Kawamura discloses at column 2, lines 9-13 that the improved circuit provides the advantage that stereo separation is maintained, even under low field-strength conditions.

It would have been obvious to one of ordinary skill in the art at the time the present invention was made to modify the decoder of Vogt et al. by providing dynamically and separately controlled "fifth" and "sixth" low-pass filters to vary the bandwidth of the demodulated audio signals, operating upon the sum and difference signals, respectively, depending upon received signal conditions according to the teachings of Kawamura, in order to minimize the effects of received noise with minimal loss of desired high frequency content and stereo separation. (In this and the following rejections, the use of quoted numbers, such as "first", "third", etc., in referring to elements of the prior art indicates correspondence to the language of Applicant's claims, not to a count of such elements in the prior art; e.g., although a prior art reference may teach only two filters, one of those may be referred to as a "fourth" filter, in order to

make clear the correspondence to a "fourth filter" recited by Applicant.)

24. Regarding **claims 18 and 21**, the decoder of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above with regard to claim 1, performs the method claimed in normal operation and thus renders the claimed method obvious. (It is noted that elements may be enumerated differently; e.g., the "fifth" and "sixth" low-pass filters of claim 1 are referred to as "first" and "second" low-pass filters, respectively in claim 21.)

25. Regarding **claim 25**, as all the limitations of this claim are contained in claim 1 (except that elements may be enumerated differently; e.g., the "fifth" and "sixth" low-pass filters of claim 1 are referred to as "first" and "second" low-pass filters, respectively in claim 25), this claim is rendered obvious by the combination of references recited above with regard to claim 1 by the same reasoning.

26. Regarding **claim 2**, Vogt et al. disclose at column 3, lines 66-67 that the at least one trigonometric function (G38s and G38c) includes a sine function and a cosine function; the same remains true in the decoder modified according to the teachings of Noeske et al., Eory, and Kawamura as described above regarding claim 1.

27. Regarding **claims 3 and 4**, Vogt et al. disclose in Fig. 1 and at column 4, lines 18-26 that the predetermined value at multiplier (15) is a cosine value retrieved from a table (16).

28. Regarding **claim 5**, in the decoder of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above regarding claim 1, the useful bandwidth of each of the low-pass filtered and decimated signals from the "first", "second", and "third" decimators are all substantially 0-15 kHz; also, Noeske et al. disclose at column 3, lines 46-49 that because the decimated sum (L+R) and difference (L-R) signals must be combined to recover the L and R signals, the decimation filters must 19 and 40 must have identical characteristics. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to low-pass filter each of the three signals to this bandwidth (15 kHz) and decimate them accordingly to the same sampling rate (at least 30k samples per second), according to this teaching of Noeske et al. and common knowledge in the art.

29. Regarding **claim 6**, assuming that this claim intends to claim the same "second decimator" recited at lines 21-23 of claim 1 (see 35 USC § 112, first and second paragraph rejections of this claim, above), this limitation (as best understood) is addressed above under claim 1.

30. Regarding **claim 16**, in the system of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above regarding claim 1, although it was generally known in the art at the time the present invention was made the sampling frequency can be reduced as low as twice the frequency of the highest-frequency component in a given signal, (140 S/s for the decimators 19 and 20 of Fig. 1 of Vogt et al. in view of the bandwidth of filters 17 and 18 [70 Hz] as described at column 4, lines 26-36 of Vogt et al.), one of ordinary skill in the art would recognize that a significantly higher sampling rate would be preferred in order to convey the necessary phase angle information required to provide a relatively smooth phase correction (phase rotation) of the quadrature pair of signals Imr1 and Imr2 at multipliers 4 and 5. A sampling frequency range of about 4 to 100 times the expected maximum output frequency of the phase angle estimation circuit (21) (140 Hz, since circuit 21 doubles the input frequency) would seem reasonable, corresponding to a sampling frequency range of about 560 S/s to 14 kS/s. Given the disclosed input sampling rate of 228 kS/s in the decoder of Vogt et al., this corresponds to a sampling rate decimation factor in the range of 16 to 407. The obviousness or advantage of any particular decimation factor depends directly upon the initial sampling rate, which is not specified in the claims of the current invention. Since the decimation factor required to achieve a desired target sampling rate depends upon the sampling rate of the applied input signal, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to select any appropriate sampling rate decimation factor to provide a suitable phase angle resolution in the phase angle estimation means (21) depending upon the

sampling rate of the applied input signal. Given the input sampling rate of 228 kS/s, specified by Vogt et al., a conservative factor of 20 would be reasonable, and selecting such a factor would have been obvious to one of ordinary skill in the art at the time the present invention was made.

31. Regarding **claim 8**, in the decoder of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above regarding claim 1, the means for using the sum and difference signals comprises combining circuitry (7, 8, and 9 of Vogt et al., equivalent to stereophonic demodulation circuit 4 of Kawamura), coupled to the "fifth" low-pass filter (first high-cut filter 2 of Kawamura) and the "sixth" low-pass filter (second high-cut filter 5 of Kawamura), said combining circuitry combining the "fifth" low-pass filter output and the "sixth" low-pass filter output to produce the left and right channel signals; and control circuitry (high-cut control circuit 8 and separation control circuit 5A of Kawamura) coupled to the "fifth and the "sixth" low-pass filters for modifying bandwidth of the "fifth" low-pass filter and the "sixth" low-pass filter in response to received signal conditions. Vogt et al. discloses at column 5, lines 18-28 that the control circuitry (22), which modifies the amplitude of the difference signal to reduce stereo separation and also noise in response to received signal conditions in the original decoder may be constructed according to the disclosure of U.S. Patent application Ser. No. 08/215,186 (now US Patent No. 5,673,324 to Kässer et al.), incorporated by reference in Vogt et al. The circuit disclosed in Fig. 1 of Kässer et al. includes a symmetry detector (11) which detects asymmetry in the 38-kHz DSBSC

(double-sideband suppressed-carrier) modulated difference signal and a high-pass detector (10) which detects high-frequency distortion caused by conditions such as multipath reception and, according to the detection of these conditions, influences an output signal "D" at 26 to indicate a reduced quality of the received signal. Official notice is taken that it was well known in the art at the time the present invention was made that adjacent channel interference in a received FM signal typically causes a lack of symmetry between the received subcarrier sidebands of the received signal. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to utilize the more advanced control circuitry of Kässer et al. to implement each of high-cut control circuit 8 and separation control circuit 5A, rather than the simple RF signal strength detector circuits taught by Kawamura, in the decoder of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura in order to provide a decoder with an automatic reception control that is responsive to the presence of adjacent signal interference and distortion of the input signal, rather than simply RF signal strength.

32. Regarding **claims 9 and 10**, Official notice is taken that the use of finite impulse response (FIR) filters in digital signal processing systems was notoriously well known in the art at the time the present invention was made, the corresponding counterpart filter classification being infinite impulse response (IIR) filters. It was further well known to modify the response characteristics (such as bandwidth) of an FIR by varying the filter coefficients. It would have been obvious to one of ordinary skill in the art at the time the

present invention was made to implement the variable-low-pass filters as taught by Kawamura as FIR filters in the decoder of Vogt et al., since the system is implemented as a digital signal processor (column 5, lines 32-38), and to modify the bandwidths of the filters by varying the filter coefficients as was common in the art.

33. Regarding **claim 11**, Vogt et al. disclose that the system is used for decoding a multiplex signal in a stereo receiver of VHF/FM stereo broadcasting (column 1, lines 18-23 and column 3, lines 3-6). (Also, see objection to this claim above.)

34. Regarding **claims 12 and 13**, [the frequency of] the predetermined "value" [function] of Fig. 1 of Vogt et al. that is multiplied by the input signal at multiplier 370 is nominally 19 kHz, the same as the nominal frequency of the pilot signal component in the input signal; however since it is independently generated in a free-running oscillator, [its frequency] is approximate to, but not equal to, a frequency of the pilot signal component in the input signal and within 3 kHz (probably within a few Hz) of the frequency of the pilot. (See 35 USC § 112, first paragraph rejection of claim 12, above.)

35. Regarding **claim 15**, as indicated above regarding claim 1, Vogt et al. do not disclose a first decimator reducing the sampling rate of a first filter output as claimed in claim 1. However, Noeske et al. do include such a combination (in element 19 of Fig. 2), and generally teach decimating all signals "to the greatest possible extent" (column 4, lines 39-41). Moreover, Noeske et al. do not disclose any particular decimation factor

used in any of the disclosed decimation filter stages. What decimation factor is practical depends directly upon the sampling rate input to the decimator, which is not specified in the claims of the present invention. Vogt et al. disclose at column 3, lines 31-33 an "advantageous" input sampling rate of 228 kHz; Noeske et al. disclose at column 4, lines 17-20 that the input signal to the decoder (mpx1) is sampled at a rate that lies within a wide range, between 100 kHz and up to a few MHz. It was notoriously well known in the art at the time the present invention was made to decimate a signal by a factor that is the largest integer that divides the input sampling rate to provide an output (decimated) sampling rate that is greater than or equal to twice the frequency of the highest-frequency desired component of the signal where a maximum degree of decimation is desired (according to the sampling theorem). Given an input sampling frequency of 228 k·S/s, as disclosed by Vogt et al., a decimation factor of no more than 7, which would yield an output sampling rate of approximately 32.6 kHz or higher to accommodate the sum (L+R) signal bandwidth of 15 kHz. Similarly, given an input sampling rate in the range of 100 kHz (k·S/s) to say 3 MHz (M·S/s), as disclosed by Noeske et al., a decimation factor of between 3 or less (corresponding to an input sampling rate of 100 k·S/s) and 100 (corresponding to an input sampling rate of 3 M·S/s), depending on the particular input sampling rate selected from that range would be obvious; given an input sampling rate of 240 k·S/s, as disclosed (but not claimed) by Applicant, a decimation factor of 8 or more is obvious. Other factors, such as selecting a widely-used "standard" sampling rate to provide compatibility with other digital audio processing systems may also affect the selection of a decimation factor in an obvious

way; however, Applicant has not disclosed any particular advantage or new or unexpected result due to employing the particular decimation factor of 5, especially with respect to an unspecified (in the claims) input sampling rate. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to decimate the signals to whatever degree practical while maintaining the required intelligence depending upon a particular input sampling rate.

36. Regarding **claim 17**, in the system of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above regarding claim 1, the phase angle estimation means (21) operates at a frequency less than one tenth a frequency of the input frequency. (The frequency-reduced pilot is nominally at 0 Hz, probably a few Hz at maximum, which is less than one tenth the predetermined frequency of the pilot at the input, 19 kHz; and the sampling frequency would be reduced to as low as 280 S/s, in view of the bandwidth of filters 17 and 18, 70 Hz as disclosed at column 4, lines 26-36 of Vogt et al., and the frequency doubling performed by the phase locked loop in the modification of the decoder of Vogt et al. described above regarding claim 1, as further described above regarding claim 16, which is less than one tenth the predetermined sampling frequency of the input signal, 228 k·S/s).

37. Regarding **claim 19**, Vogt et al. do not teach adding a predetermined phase correction to a phase value of the intermediate signal to produce a resultant phase value, wherein the predetermined phase correction is a function of a delay of a portion

of the digital circuitry. Noeske et al. disclose in Figs. 2 and 4 and describe at column 4, lines 34-38 correction values k1, k2, and k3 that are applied to correcting devices 16, 23, and 33 to correct for system-inherent delays. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to include these elements (and inherent method steps) in the decoder and inherent method of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above, as one of ordinary skill in the art would have recognized that such delays would also be present in such a combination.

38. Regarding **claim 20**, Noeske et al. disclose in Figs. 2 and 4 and describe at column 3, lines 28-36 and lines 54-61 frequency multipliers 22 and 32, which multiply the phase value (φ) generated by PLL 10 by predetermined positive integers to produce multiplied result and phase values and provides trigonometric values of the multiplied phase values. In the decoder formed by combining the teachings of Vogt et al., Noeske et al., Eory, and Kawamura as described above regarding claims 1 and 21, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply this teaching by multiplying the phase value generated by the 19-kHz pilot carrier tracking phase-locked loop by a factor of two (according to the teachings of Noeske et al.) and providing first and second trigonometric functions (frequency-doubled quadrature-phased PLL output pair) by determining first and second trigonometric values (sine and cosine) of the resultant phase according to the combined teachings of Noeske et al. and Eory.

39. Regarding **claim 22**, Vogt et al. do not disclose the particular implementation of the filters in the decoder. Official notice is taken that the use of finite impulse response (FIR) filters in digital processing systems was notoriously well known in the art at the time the present invention was made, the corresponding counterpart filter classification being infinite impulse response (IIR) filters. FIR filters are often preferred over IIR filters because they have linear phase responses (with symmetrical coefficients) and are always stable, whereas IIR filters are not guaranteed stable and never have linear phase responses. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the filtering processes in the decoder of Vogt et al., modified according to the teachings of Noeske et al., Eory, and Kawamura as described above regarding claims 1 and 21, as one or more FIR filters, since the system is implemented as a digital signal processor (column 5, lines 32-38).

40. Regarding **claim 23**, Vogt et al. discloses at column 5, lines 32-38 that the decoder may be implemented by suitable programming (in software, inherently) of a digital signal processor; thus, the filtering would be performed in software.

41. Regarding **claim 24**, in the software programmed DSP system of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claims 1 and 21, the filter coefficients would inherently be software modifiable.

Response to Arguments

42. Applicant's arguments, see page 12, lines 8-13, filed 6 October 2004, with respect to the rejection of **claim 8** under 35 USC 112, first paragraph have been fully considered and are persuasive. The rejection of claim 8 under 35 USC 112, first paragraph has been withdrawn.

43. Applicant's arguments, see page 12, line 14-18, filed 6 October 2004, with respect to the rejection of **claim 1** under 35 USC 112, second paragraph have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of a lack of enablement for the full scope of the claim (35 USC 112, first paragraph) and a lack of antecedent basis in the claim for the limitation "the sixth low pass filter that processes the output signal containing a difference of left channel information and right channel information" (35 USC 112, second paragraph).

44. Applicant's arguments with respect to **claims 1-6, 8-13, 16-19, and 21-25** under 35 USC § 103(a) have been considered but are moot in view of the new ground(s) of rejection.

45. New references Noeske et al. and Eory have been found, which teach phase-locked loop phase estimator elements and methods in radio receivers that combine with previously applied references Vogt et al. and Kawamura to show the presently amended claims to be obvious.

46. Applicant's arguments with respect to **claims 14, 15, 19, and 20** under 35 USC § 103(a) have been considered but are moot in view of the new ground(s) of rejection.

47. New references Noeske et al. and Eory in combination with previously applied references Vogt et al. and Kawamura teach the additional limitations of these claims and render the additional references Patel et al. and Whikehart et al. unnecessary in rejecting the present claims. Thus, Applicant's arguments with respect to Patel et al. and Whikehart et al. are essentially moot.

Conclusion

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

49. Wildhagen (EP 1094613 A1) discloses a digital stereo multiplex decoder which employs extensive decimation of signals and a digital phase locked loop for locking to the phase and frequency of a pilot signal and generating a synchronized carrier signal to demodulate a difference signal component.

50. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony M Jacobson whose telephone number is 571-272-7521. The examiner can normally be reached on M-F 11:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh N Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tmj
April 19, 2005

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SUPERVISORY PATENT EXAMINER